ABSTRACT OF THE DISCLOSURE

A test circuit and method are disclosed for testing memory cells of a ferroelectric memory device having an array of ferroelectric memory cells. The test circuitry is coupled to the bit lines, for selectively determining the voltage levels appearing on the bit lines based on a measured current level and providing externally to the ferroelectric memory device an electrical signal representative of the sensed voltage levels. In this way, ferroelectric memory cells exhibiting degraded performance may be identified.